

# Rohit Suryadevara

Burlington, ON | Canadian Citizen

rohit.suryadevara.661@gmail.com | linkedin.com/in/RohitSuryadevara | github.com/rohit661x

## EDUCATION

---

### McMaster University

*Bachelor of Science in Mathematics, Minor in Finance*

Sept 2024 – April 2027

Hamilton, ON

**Relevant Coursework:** Probability and Stochastics (Masters Audit), Applications of Machine Learning, Data Structures & Algorithms, Software System Design, Probability, Statistics, Calculus

## TECHNICAL SKILLS

---

- **Languages:** Python, C/C++, SQL, R, Bash, JavaScript/TypeScript, HTML, CSS
- **ML & Data:** PyTorch, TensorFlow, Scikit-learn, XGBoost, Pandas, NumPy, Hugging Face, LangChain
- **DevOps/Platforms:** Git, Docker, Kubernetes, Kafka, Terraform, Ansible, GitHub Actions, Jenkins, GitLab
- **Cloud/Databases:** PostgreSQL, MongoDB, Supabase, MySQL, SQLite, Redis, AWS, Azure, Google Cloud

## PROFESSIONAL EXPERIENCE

---

### Artificial Intelligence Developer

*IG Wealth Management — Mortgage, Insurance & Banking*

May 2026 – August 2026

- Built an **agentic framework** hosted on **GCP** using **Pub/Sub**, **Dataflow**, and **BigQuery** orchestrated via **Gemini Enterprise Agents** alongside deterministic custom models for regulatory-compliant automation, reducing standardized mortgage review by **90%** and saving **400–500 hours monthly**.
- Engineered production guardrails that **reduced API costs by 60%** via **Vertex AI Vector Search** semantic caching, automated **PII masking** using **Cloud DLP**, and deployed **Vertex AI Pipelines** for continuous hallucination tracking.
- Shipped POC-to-production **agentic workflows** under **MLOps** and **agile** frameworks while managing technical governance documentation and strategic alignment presentations for the MIB division.

### Research Member — Safety & Alignment

*Cohere Labs Open Science Community*

March 2026 – Present

- Engineered **MAP**, a **black-box LLM attribution** framework to classify **13 frontier model families** and quantify **prompt injection** risks via behavioral feature extraction; presented findings at the **Canadian Statistical Student Conference** (May 2026).
- Developed automated **PyTorch**-based evaluation pipelines to stress-test black-box behaviors, establishing rigorous **red-teaming** methodologies and **guardrail validation** benchmarks for deployment-facing GenAI systems.
- Expanded guardrail robustness via **multilingual safety benchmarking**, evaluating **reward model vulnerabilities**, **cross-cultural prompt injections**, and toxic generation risks across **low-resource languages** for open-source community releases.

### Software Engineer

*Arkimetrix Analytics*

Sept 2025 – Dec 2025

- Reduced manual processing by **70%+** across **10K+ records** by building document parsing pipelines via **Azure Form Recognizer**, **Google Gemini API**, and **Docker** with **containerized CI/CD** and schema enforcement.
- Cut end-to-end reporting latency by **90%** (minutes → **sub-30 seconds**) by optimizing **Flask/PostgreSQL** APIs and **ETL pipelines** via **CRON jobs** for month-end batch processing.

### Machine Learning Researcher

*McMaster University — Faculty of Engineering*

May 2025 – Aug 2025

- Achieved **4x faster** pattern recognition on **100GB+** genomic datasets by engineering novel overlapping position algorithms to eliminate sequential bottlenecks in the **MAXCOVER** protein sequence pipeline.
- Eliminated reproducibility gaps by building automated testing infrastructure with **GitHub Actions**, **PyTorch**, and **MLflow**; benchmarked latency and throughput across experimental workflows for consistent model validation.

## EXTRACURRICULAR EXPERIENCE

---

### AI Research Project Member

June 2026 – Present

*McMaster Artificial Intelligence Society (MacAI) — CUCAI 2027*

- Building a **multimodal deep learning** system to classify thoracic abnormalities and estimate severity from **chest X-rays**, generating **saliency heatmaps (Grad-CAM)** for explainable localization of model predictions.
- Developing a **vision-language pipeline** to produce radiology-style diagnostic reports from imaging features; advancing the project from research to a presented system at the **Canadian Undergraduate Conference on AI (CUCAI) 2027**.

### Project Lead

April 2026 – May 2026

*Greypoint Industries — DND IDEaS Counter-Drone Contract Bid (\$200,000)*

- Architected a **Bayesian/Kalman** multi-modal sensor fusion model for a **DND IDEaS** counter-drone proposal, fusing **RF/EW telemetry**, **visual-inertial kinematics**, and operational context through a **soft-switching anti-spoof gate** for resilient tracking in **GPS/RF-contested** environments.
- Sustained track continuity under individual sensor dropout via **dynamic confidence reweighting** across heterogeneous inputs; designed for edge deployment within **SWaP** constraints; submitted as a \$200K competitive bid.

### DevOps Engineer (Volunteer)

Jan 2026 – April 2026

*DEFEND — 65square (Nonprofit, Online Safety Platform)*

- Streamlined release automation by engineering **CI/CD pipelines** with **GitLab CI/CD**, building and pushing **Docker** container images to **AWS**.
- Standardized dependency management and dev/prod parity by migrating back-end services into isolated **Docker** containers.
- Restored platform reliability by leading **Level 2 incident response**, performing **RCA** on service failures, and deploying automated pipeline fixes.

## PROJECTS

---

### Neuroplasticity-Inspired Deep Learning Optimizer | *Python, PyTorch, TensorFlow*

- Achieved **52% model sparsity** while maintaining **98% accuracy** on MNIST by implementing custom deep learning optimizer with dynamic sparsity regularization for neural network compression
- Designed meta-learning experimentation framework to evaluate learning rate schedules and structural constraints, demonstrating ML algorithm development and hyperparameter optimization

### Bare-Metal Monolithic Kernel Operating System for Low Latency Trading | *C, x86 Assembly, Verilog*

- Designed a bare-metal trading kernel that eliminates OS-level latency sources (interrupts, syscalls, context switches) to achieve **sub-microsecond decision-to-trade latency** for single-security execution in emulation
- Engineered a DMA-driven receive path with inline x86 MMIO, a Verilog RTL NIC parser, and cache-line-aligned structures within **L2 residency**, which was tuned under KVM with core isolation and SMT disabled